At page 16, line 6, please delete "optical" and insert --operation-- in place thereof.

At page 17, line 11, please delete "output" and insert --outputs-- in place thereof.

IN THE CLAIMS:

Please amend claims 1, 2, 4-9, 18 and 19 as follows:

1. (Amended) A method of controlling a flash memory system comprising the steps of:

modifying [the] data of a group of [memory units, each having a plurality of] flash memory cells adapted to erasing data therefrom and writing data therein;

checking for the presence or absence of an error of not properly modifying said data of said group of memory units; and

determining the completion of proper modification of said data of said group of memory units provided that an error is detected and said error can be corrected.

2. (Amended) A method of controlling a flash memory system comprising steps of:

erasing [the] data written in a group of [memory units, each having a plurality of] flash memory cells adapted to erasing data therefrom and writing data therein;

reading the data written in said group of memory units having said data erased and checking the completion of proper erasure of said data;

counting the number of errors of not being properly erased provided that said data are not properly erased as a result of said checking step; and

determining [the] completion of proper erasure of said data of said group of memory units provided that the counted number of errors is within a correctable range.

4. (Amended) A flash memory system comprising:

a group of memory units, each having a plurality of flash memory cells adapted to erasing data therefrom and writing data therein;

B2 Cont. an error detection[/correction] unit for reading the data written in said group of memory [unit] units and detecting[/correcting] errors [up to a predetermined number]; and

an error judgement section for counting the number of errors detected by said error detection[/correction] unit and determining the completion of proper data modification of data provided that the number of errors detected by said error detection[/correction] unit is not greater than [said predetermined] a number which can be corrected in accordance with an error check code.

5. (Amended) A flash memory system comprising:

a memory cluster having a plurality of flash memory cells adapted to erasing data therefrom and writing data therein;

at least one or more than one memory sectors constituting said memory cluster;

a flash memory control unit for ordering erasure of the data written in said memory cluster;

an error detection/correction unit for detecting erase errors in the data read from said memory cluster and correcting erase errors up to n (n is a number of memory cells in a memory sector, that can be corrected in accordance with an error check code) attribute to memory cells; and

an error judgement section for counting the erase errors of each memory sector and determining the completion of proper data erasure provided that the completion of proper data erasure provided that the number of memory cells storing unerased data is not greater than m ($1 \leq m \leq n$) in each and every memory sector.

6. (Amended) A flash memory system comprising:

a memory cluster having a plurality of flash memory cells adapted to erasing data therefrom and writing data therein;

at least one or more than one memory sectors constituting said memory cluster;

a flash memory control unit for ordering erasure of the data written in said memory cluster;

an error detection/correction unit for detecting erase errors in the data read from said memory cluster and correcting erase errors up to n (n is a number of symbols in a memory sector that can be corrected in accordance with an error check code (1 symbol = k bits, k≥2)) symbols [(1 symbol = k bits, k≥2)] attributable to the data;

a counter unit for counting the number of symbols showing erase errors and contained in each memory sector; and

an error judgement section for determining the completion of proper data modification provided that the number of symbols showing erase errors is not greater than m ($1 \leq m \leq n$) in each and every memory sector.

7. (Amended) A flash memory system comprising:

a memory cluster comprising a plurality of external flash memory cells;

at least one or more than one memory sector constituting said memory cluster;

a flash memory control unit for ordering writing of the data in said memory sectors;

an error detection/correction unit for detecting errors in the data read from said memory cluster and correcting erase errors up to n (n is the number of memory cells in a memory sector, that can be corrected in accordance with an error check code) attributable to flash memory cells; and

an error judgement section for counting the number of memory cells defective in terms of writing and contained in each memory sector and determining the completion of proper data writing provided that the number of memory cells defective in terms of writing is not greater than n in each and every memory sector.

8. (Amended) A flash memory system comprising:

memory sectors having a plurality of flash memory cells;

a flash memory control unit for ordering writing of the data in each of said memory sectors;

an error detection/correction unit for detecting write errors in the data read from said memory cluster and correcting write errors up to n (n is a number of symbols in a memory sector, that can be corrected in accordance with an error check code (1 symbol = k bits, k≥2) symbols (1 symbol = k bits, k≥2) attributable to the data ;

an error judgement section for counting the number of symbols defective in terms of writing as detected by said detection unit aid and determining the completion of proper data modification provided that the number of symbols showing errors is not greater than m (1≤m≤n) in each and every memory sector.

9. (Amended) A flash memory system comprising:

a memory cluster comprising a plurality of external flash memory cells;

at least one or more than one memory sectors constituting said memory cluster;

a flash memory control unit for ordering writing of the data in said memory sectors;

an error detection/correction unit for detecting write errors in the data read from said memory cluster and correcting write errors up to n (n is a number of bits in a memory sector, that can be corrected in accordance with an error check code) bits attributable to the data; and

an error judgement section for counting the number of bits showing write errors and determining the completion of proper data writing provided that the number of bits showing write errors is not greater than m ($1 \leq m \leq n$) bits in each and every memory sector.

18. (Amended) A flash memory device comprising:

a group of memory units, each having a plurality of flash memory cells adapted to erasing data therefrom and writing data therein; and

an error judgement section for determining the completion of proper data modification of data provided that the number of errors detected by an error detection/correction unit detecting/correcting errors in the data written in said group of memory units is not greater than a [predetermined] number of errors within a correctable range.

19. (Amended) a flash memory device comprising:

a group of memory units, each having a plurality of flash memory cells adapted to erasing data therefrom and writing data therein;

an error detection[/correction] unit for reading the data [written in] from said group of memory [unit] units and detecting[/correcting] errors [up to a predetermined number]; and

an error judgement section for counting the number of errors detected by said error detection[/correction] unit and determining the completion of proper data modification of data provided that the number of errors detected by said error detection[/correction] unit is not greater than [said predetermined] a number which can be corrected in accordance with an error check code.

Please add new claims 23-30 as follows:

--23. A flash memory system comprising:

a flash memory cell array;

a control circuit for erasing data from designated part of said memory cell array, for writing data into given part of said memory cell array, and for reading data from said designated or given part of said memory cell array, thereby it can be detected how many errors have been occurred within said designated or given part of said memory cell array after erasing or writing;

a counter for counting the number of the errors based on data read by said control circuit after the erasing or writing;

an error judgement section for outputting information that it is successfully erased or written if the number counted is smaller than a number which can be corrected in accordance with an error check code; and

an error detection/correction unit equipped beside said counter and said error judgement section for generating said error check code accompanying with data to be written into said given part of said memory cell array, said error check code being also written into said given part, and for correcting errors existing in data read from said designated or given part of said memory cell array.

24. The flash memory system according to claim 23, wherein said number can be corrected in accordance with an error check code, that is one.

25. The flash memory system according to claim 23, wherein data stored in said memory cell array is divided into a plurality of symbols (1 symbol = k bits; k>0), said counter counts the number of the errors in increments of one of said symbols, and if any one bit among one symbol is failed in erasing or writing, said counter assumes that such symbol is an error.

26. The flash memory system according to claim 25, wherein said number that can be corrected in accordance with an error check code is one.

27. A flash memory device comprising:

a flash memory cell array;

a control circuit for erasing data from designated part of said memory cell array, for writing input data and check code incidental to said input data into given part of said memory cell array, said input data being also input from external, and for reading data from said designated or given part of said memory cell array, thereby it can be detected how many errors have been occurred within said designated or given part of said memory cell array after erasing or writing;

a counter for counting the number of the errors based on data read by said control circuit after the erasing or writing; and

an error judgement section for outputting information that it is successfully erased or written if the number counted is smaller than a number can be corrected in accordance with an error check code;

wherein if read instruction and address are input to the flash memory device, the input data and the check code stored in part of said memory cell array addressed by said address are read out by said control circuit and output to external without any modification.

28. The flash memory device according to claim 27, wherein said number that can be corrected in accordance with an error check code within a correctable range is one.

29. The flash memory device according to claim 27, wherein data stored in said memory cell array is divided into a plurality of symbols (1 symbol = k bits; k>0), said counter counts the number of the errors in increments of one of said symbols, and if any one bit among one symbol is failed in erasing or writing, said counter assumes that such symbol is an error.